CLAIMS

1. A method of routing an integrated circuit (IC) design, comprising:

accessing the IC design including a plurality of objects on one or more layers;

forming a plurality of levels, wherein the plurality of levels includes a first level representing the IC design at a first grid density, a second level representing the IC design at a second grid density finer than at least the first grid density, and a third level representing the IC design at a third grid density finer than at least the first grid density and the second grid density;

based at least partly on the IC design, populating each level of the plurality of levels with the plurality of objects; and

interconnecting the objects at one or more of the first level, the second level, and the third level.

2. The method of claim 1, wherein the routing is multithreaded at least at a first time.

3. The method of claim 1, wherein the routing is single threaded at least at a first time.

4. The method of claim 1, wherein each of the IC design, the first level, the second level, and the third level include at least two layers.

5. The method of claim 1, wherein each of the IC design, the first level, the second level, and the third level include one layer.

6. A method of routing an integrated circuit (IC) design, comprising:

accessing the IC design including a plurality of objects on one or more layers;

accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of one or more partitions, and the plurality

of objects of the IC design are among the first plurality of one or more partitions; and

forming a second level for the IC design, including:

partitioning the second level into a second plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions; and

within each partition of the second plurality of partitions, interconnecting objects substantially independently of other partitions of the second plurality of partitions.

7. The method of claim 6, wherein the routing is multithreaded at least at a first time.

8. The method of claim 6, wherein the routing is single threaded at least at a first time.

9. The method of claim 6, wherein one or more partitions of the first plurality of one or more partitions has no objects of the plurality of objects.

10. The method of claim 6, wherein every partition of the first plurality of one or more partitions has one or more objects of the plurality of objects.

11. The method of claim 6, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the second plurality of partitions.

12. The method of claim 6, wherein interconnecting objects substantially independently is subject at least to a first partition of the second plurality of partitions locking at least a net shared by at least the first partition and a second partition of the second plurality of partitions to prevent a change of the net by the second partition of the second plurality of partitions.

13. The method of claim 6, wherein each partition of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions.

14. The method of claim 6, wherein each of the IC design, the first level, the second level, and the third level include at least two layers.

15. The method of claim 6, wherein each of the IC design, the first level, the second level, and the third level include one layer.

16. A method of routing an integrated circuit (IC) design, comprising:

accessing the IC design including a plurality of objects on one or more layers;

accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of one or more partitions, and the plurality of objects of the IC design are among the first plurality of one or more partitions; and

forming a second level for the IC design, including:

partitioning the second level into a second plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions;

allotting the second plurality of partitions among a plurality of areas, such that each area of the plurality of areas includes one or more partitions of the second plurality of partitions; and

within each area of the plurality of areas, interconnecting objects substantially independently of other areas of the plurality of areas.

17. The method of claim 16, wherein the routing is multithreaded at least at a first time.

18. The method of claim 16, wherein the routing is single threaded at least at a first time.

19. The method of claim 16, wherein one or more partitions of the first plurality of one or more partitions has no objects of the plurality of objects.

20. The method of claim 16, wherein every partition of the first plurality of one or more partitions has one or more objects of the plurality of objects.

21. The method of claim 16, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the second plurality of partitions.

22. The method of claim 16, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the plurality of areas.

23. The method of claim 16, wherein interconnecting objects substantially independently is subject at least to a first partition of the second plurality of partitions locking at least a net shared by at least the first partition and a second partition of the second plurality of partitions to prevent a change of the net by the second partition of the second plurality of partitions.

24. The method of claim 16, wherein interconnecting objects substantially independently is subject at least to a first area of the plurality of areas locking at least a net shared by at least the first area and a second area of the plurality of areas to prevent a change of the net by the second area of the plurality of areas.

25. The method of claim 16, wherein each of the IC design, the first level, the second level, and the third level include at least two layers.

26. The method of claim 16, wherein each of the IC design, the first level, the second level, and the third level include one layer.

27. A method of routing an integrated circuit (IC) design, comprising:

accessing the IC design including a plurality of blockages and a plurality of pins;

forming a graph including a first plurality of nodes, wherein each node of the first plurality of nodes is formed outside every blockage of the plurality of blockages; and

interconnecting the plurality of pins through nodes of the graph.

28. The method of claim 27, wherein the routing is multithreaded at least at a first time.

29. The method of claim 27, wherein the routing is single threaded at least at a first time.

30. A method of routing an integrated circuit (IC) design, comprising:

forming a first plurality of nodes for positioning objects of the IC design in a first layer, wherein at least two nodes of the first plurality of nodes are spaced apart by a first interval; and

forming a second plurality of nodes for positioning objects of the IC design in a second layer, wherein at least two nodes of the second plurality of nodes are spaced apart by the first interval, and at least two nodes of the second plurality of nodes are spaced apart by one or more intervals greater than the first interval.

31. The method of claim 30, wherein the routing is multithreaded at least at a first time.

32. The method of claim 30, wherein the routing is single threaded at least at a first time.

33. A method of routing an integrated circuit (IC) design, comprising:

forming a first plurality of nodes for positioning objects of the IC design in a first layer, wherein at least two nodes of the first plurality of nodes are spaced apart by a first interval; and

forming a second plurality of nodes for positioning objects of the IC design in a second layer, wherein at least two nodes of the second plurality of nodes are spaced apart by the first interval, and at least two nodes of the second plurality of nodes are spaced apart by one or more intervals less than the first interval.

34. The method of claim 33, wherein the routing is multithreaded at least at a first time.

35. The method of claim 33, wherein the routing is single threaded at least at a first time.

36. A method of routing an integrated circuit (IC) design, comprising:

forming a first plurality of nodes for positioning objects of the IC design in a first layer, wherein the first plurality of nodes includes a first plurality of common nodes and a first plurality of uncommon nodes; and

forming a second plurality of nodes for positioning objects of the IC design in a second layer,

wherein the second layer is at least substantially parallel to the first layer and the second layer is spaced apart from the first layer by about a layer distance along a layer axis,

and wherein the second plurality of nodes includes a second plurality of common nodes, the first plurality of common nodes and the second plurality of common nodes share positions, such that if the second plurality of common nodes were shifted toward the first plurality of common nodes by about the layer distance

along the layer axis, the first plurality of common nodes and the second plurality of common nodes would be substantially identical,

and wherein if the second plurality of common nodes were shifted toward the first plurality of uncommon nodes by about the layer distance along the layer axis, no node of the first plurality of uncommon nodes and no node of the second plurality of common nodes would be substantially identical.

37. The method of claim 36, wherein the routing is multithreaded at least at a first time.

38. The method of claim 36, wherein the routing is single threaded at least at a first time.

39. The method of claim 36, wherein each of the IC design, the first level, the second level, and the third level include at least two layers.

40. The method of claim 36, wherein each of the IC design, the first level, the second level, and the third level include one layer.

41. A method of routing an integrated circuit (IC) design, comprising:

defining a volume of the IC design, wherein a subset of the volume carries wiring; and

forming a plurality of nodes in the volume, wherein nodes of the plurality of nodes are limited to being formed within the subset of the volume.

42. The method of claim 41, wherein the routing is multithreaded at least at a first time.

43. The method of claim 41, wherein the routing is single threaded at least at a first time.

44. The method of claim 41, wherein the volume includes one layer.

45. The method of claim 41, wherein the volume includes at least two layers.

46. A method of routing an integrated circuit (IC) design, comprising:

accessing one or more routing pitches of one or more layers of the IC design;

defining a volume of the IC design, wherein a subset of the volume carries wiring;

forming a first plurality of nodes in the volume; and

forming a second plurality of one or more nodes outside the volume, wherein at least one node of the second plurality of one or more nodes is formed at a pitch greater than at least one of the one or more routing pitches.

47. The method of claim 46, wherein the routing is multithreaded at least at a first time.

48. The method of claim 46, wherein the routing is single threaded at least at a first time.

49. The method of claim 46, wherein the volume includes one layer.

50. The method of claim 46, wherein the volume includes at least two layers.

51. A method of routing an integrated circuit (IC) design, comprising:

accessing a first cell instance of the IC design;

accessing a second cell instance of the IC design adjacent to the first cell instance, wherein the first cell instance and the second cell instance are spaced apart by a channel;

forming a first node near a first end of the channel;

forming a second node near a second end of the channel; and

connecting a wire directly between the first node and the second node.

52. The method of claim 51, wherein the routing is multithreaded at least at a first time.

53. The method of claim 51, wherein the routing is single threaded at least at a first time.

54. A method of routing an integrated circuit (IC) design, comprising:

accessing one or more routing pitches of one or more layers of the IC design;

accessing a first cell instance of the integrated circuit design;

accessing a second cell instance of the integrated circuit design adjacent to the first cell instance, wherein the first cell instance and the second cell instance are spaced apart by a channel; and

forming a plurality of one or more nodes in the channel, wherein the plurality of one or more nodes in the channel has a pitch greater than at least one of the one or more routing pitches.

55. The method of claim 54, wherein the routing is multithreaded at least at a first time.

56. The method of claim 54, wherein the routing is single threaded at least at a first time.

57. A method of routing an integrated circuit (IC) design, comprising:

accessing the IC design including a plurality of objects;

accessing a plurality of routing algorithms;

interconnecting, with a first plurality of interconnections, one or more of the plurality of objects, at least partly in response to a first combination of one or more routing algorithms of the plurality of routing algorithms;

storing the first plurality of interconnections;

automatically determining a second combination of one or more routing algorithms;

interconnecting, with a second plurality of interconnections, one or more of the plurality of objects, at least partly in response to the second combination of one or more routing algorithms of the plurality of routing algorithms;

comparing results of the first plurality of interconnections and the second plurality of interconnections; and

if results of the second plurality of interconnections are worse than results of the first plurality of interconnections, restoring the first plurality of interconnections.

58. The method of claim 57, wherein the routing is multithreaded at least at a first time.

59. The method of claim 57, wherein the routing is single threaded at least at a first time.

60. A method of routing an integrated circuit (IC) design, comprising:

interconnecting at least a first portion of the IC design at a first routing pitch; and

if the interconnecting results in one or more design rule violations, routing at least a part of the first portion of the IC design at a second routing pitch less than the first routing pitch.

61. The method of claim 60, wherein the routing is multithreaded at least at a first time.

62. The method of claim 60, wherein the routing is single threaded at least at a first time.

63. The method of claim 60, wherein the part of the first portion of the IC design routed at the second routing pitch less than the first routing pitch includes a part of the IC design causing at least one of the one or more design rule violations.

64. A method of routing an integrated circuit (IC) design, comprising:

interconnecting at least a first part of the IC design on at least a first thread; and

interconnecting at least a second part of the IC design on at least a second thread.

65. The method of claim 64, wherein the first thread runs on at least a first processor and the second thread runs on at least the first processor.

66. The method of claim 64, wherein the first thread runs on at least a first processor and the second thread runs on at least a second processor.

67. The method of claim 64, wherein at a first time, both the first thread and the second thread run.

68. The method of claim 64, wherein at a first time, at least one of the first thread and the second thread does not run.

69. The method of claim 64, wherein 1) at a first time, both the first thread and the second thread run, and 2) at a second time, at least one of the first thread and the second thread does not run.